$L\infty$ Voronoi Diagrams and applications in VLSI Layout and Manufacturing

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Abstract

The Voronoi diagram of polygonal objects has been given considerable attention because of its numerous applications in diverse areas. In this paper we address the L_∞ Voronoi diagram of polygonal objects and present applications in VLSI layout and manufacturing.

It is well known that the ordinary Voronoi diagram of polygonal objects in the plane consists of straight line segments and parabolic arcs and its combinatorial complexity is linear in the number of vertices of the polygonal objects (see [1] for a survey). The existence of parabolic arcs however, makes it hard to compute in practice. As it was shown in [2], the Voronoi diagram of segments can be constructed with *degree*[2] 40. This is very high for practical problems involving Voronoi diagrams especially where efficiency is more important than accuracy. A practical solution to the high degree problem of the Voronoi diagram of segments may be the use of a different geometry, in particular, the L_∞-metric. An intuitive way to view the L_∞ Voronoi diagram of polygonal shapes is to view it as the locus of points corresponding to centers of isothetic squares that touch the boundary in at least two points. In contrast, the Euclidean Voronoi diagram can be regarded as the locus of centers of circles that touch the boundary in at least two points. We show that the L_∞ Voronoi diagram of polygonal objects consists of straight line segments and its combinatorial complexity is similar to the Euclidean case. If the input vertices are on rational coordinates the L_∞ Voronoi vertices are also on rational coordinates. Thus, in applications where Euclidean accuracy is not particularly important, the L_∞ Voronoi diagram of polygonal objects can provide a simpler alternative.

Our motivation for considering L_∞ Voronoi diagrams comes from applications in VLSI layout and manufacturing. The proximity information preserved in the L_∞ Voronoi diagram can be used to calculate the *critical area*, a measure used in estimating the sensitivity of a VLSI layout to defects during manufacturing of the chip. The L_∞ Voronoi diagram or medial axis can be used as a skeleton for VLSI shapes[3] which preserves proximity in the L_∞ metric, consists of straight-line segments, and whose vertices are on rational coordinates.

The yield of a VLSI chip is the percentage of functional chips among all chips manufactured. Predicting the yield of a chip before it is actually manufactured is important in order to control the cost of manufacturing. Yield estimation models are based on the concept of *critical area* which

[2]The *degree* of an algorithm is a complexity measure introduced in [5] which characterizes the complexity of the test computations of an algorithm.

[3]VLSI shapes need not be rectilinear.

represents the main computational problem in the analysis of yield loss due to spot defects during fabrication. The critical area of a layout is a measure reflecting the sensitivity of the layout to spot defects caused by particles such as dust and other contaminants in materials and equipment. In particular the critical area is defined as $A_c = \int_0^\infty A(r)D(r)dr$ where $A(r)$ denotes the area in which the center of a defect of radius r must fall in order to cause circuit failure and $D(r)$ is the density function of the defect size. Defects are usually modeled as circles and the density function has been estimated to follow the "$1/r^3$" distribution [4, 6, 7, 8]. To simplify the computation defects have often been treated as squares (e.g. [6]).

Modeling defects as squares corresponds to computing critical area in the L_∞ metric. We show that the critical area for shorts can be computed analytically once the 2nd order L_∞ Voronoi diagram of the layout is available. In particular, the critical area formula can be written as a function of the edges of the 2nd order Voronoi diagram of layout shapes. We provide a simple algorithm to compute the L_∞ Voronoi diagram of polygons by modifying the wavefront approach of [3] for points and "nice metrics". Thus, the critical area for shorts of a VLSI layout can be computed accurately in $O(n \log n)$ time assuming square defects.

Existing methods to compute critical area require substantial CPU time. They can be summarized into three categories: 1) Geometric methods, where $A(r)$ is computed for several different values of r independently and then the results are used to approximate A_c. The methods to compute $A(r)$ are usually based on *shape-expansion* followed by *shape-intersection* (see [8] for references). For rectilinear layouts there is a more efficient scan-line method [6]. 2) Monte Carlo simulation, where a large number of defects is drawn with their radii distributed according to $D(r)$. The critical area is estimated by dividing the number of defects causing faults over the total number of defects [9]. 3) Grid-based approach, where an integer grid is assumed over the layout and the critical radius (i.e., the radius of the smallest defect causing a fault at this point) of every grid point is computed.

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