



Diglog Help Session

To get started, run:
`/course/cs031/bin/diglog &`



Overview

- Starting Diglog
- Basic Diglog Usage
- Drawing Simple Circuits
- Saving and Loading
- More Diglog Editing
- Advanced Diglog Features



Starting Diglog

- Diglog is located at `/course/cs031/bin/diglog`
- Command to run is: `diglog`
 - Unless your path is set up incorrectly, talk to us if this happens
- When you run `diglog`, two windows should appear.
 - “newcrt” and “mylib”

Exiting Diglog

- **ALWAYS** use the menu Misc → Exit
- If you close the window, bad things will happen



`newcrt`

- Functions as a console where Diglog asks you administration and configuration questions.
- Always keep your newcrt window visible.
- When the mylib window stops working, often Diglog is waiting for a response in the newcrt window.
- Try moving the newcrt window to a different virtual desktop so that you can easily view it even if your mylib window is maximized.
- Turn off Num Lock. Diglog doesn't like it.



mylib

- The visual representation of your circuit.
- Actual layout and design is in this window.
- You'll do most of your work here.
- Best to maximize this window
 - Use the maximize button of your window manager
 - Manually resize the window to be larger



Drawing Wires

- Click once and move the mouse.
- Click again to place the endpoint.
- You can then continue drawing at 90 degree angles.
- Right click to stop laying wire.
- If two wires cross, click on the intersection to join them.
- To unjoin two wires, click on the intersection again.

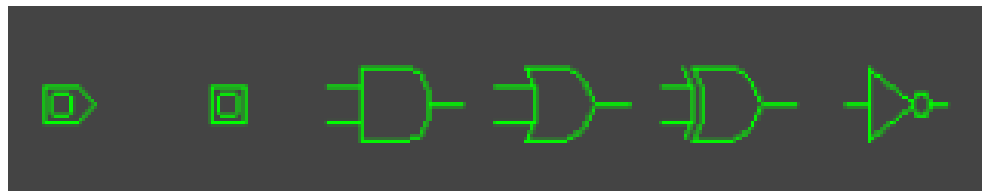


Deleting

- To delete press the `d` key.
- Your cursor will change into a pair of scissors.
- Click on what you want to delete, or click and hold to draw a box o' deletion.
- Right click to exit delete mode.



Basic Gates

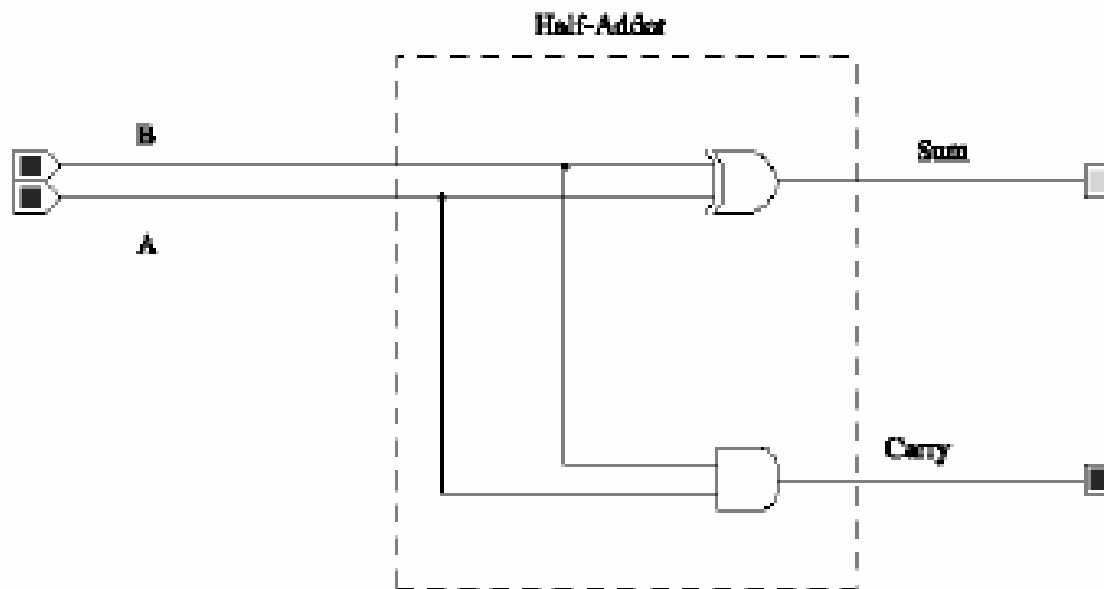


- Switch (Input) - Allows you to set a binary value to a single wire.
- LED (Output) - Shows the binary value of a single wire.
- AND, OR, XOR, INV (Gates) – Perform the specified operation on the inputs.



Half Adder Example

- Let's draw this circuit in the `mylib` window.



- Don't worry about the dashed box or labels yet.



Running the circuit

- Simulation
 - Turn on simulation (press “o” or select Misc::Simulation to test your circuit.
 - Turn it off when you are designing!
- **Warning:** Race Conditions
 - Don’t connect an on wire and an off wire or you will get a race condition.
 - Looks like flashing red and black.
 - But steady-state high-low contention is dark-red.
 - This will use up lots of CPU time and your circuit will have unpredictable (read: wrong) behavior.



Loading and Saving

- Use Misc::`Load` and Misc::`Save`
- Switch to `newcrt` window to enter filenames
- Can type in a absolute or relative filename.
 - No tildes. Very picky.
- The best thing to do is to start diglog from the directory to which you would like to save your files. Then you can just type the file's name.
- To access your home dir from another location, use `/u/<login>/course/cs031/yourfile`



Loading and Saving (cont)

- Save really, really often. Diglog can be frustrating and *there's no undo!!*
 - Did we mention there's no undo?
- Diglog files will be <filename>.lgf
- Don't forget about .snapshot either!
- Files are small, so feel free to save many versions of your work.



- Boxes
 - Use to visually group like components
 - Draw a box around the half-adder now
- Labels
 - Use like you would comments in a program
 - Always add a label with your name and login
 - Select Frills::Label. Type the text. It appears near the bottom left of the drawing window.
 - When done typing, drag the text to the location
 - Add labels to the half-adder now



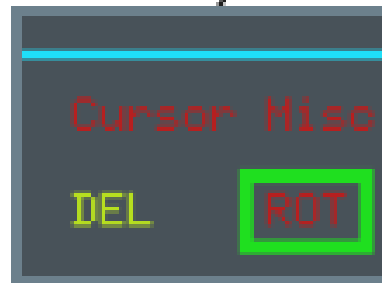
Moving the View

- The circuit drawing area is actually much larger than can be displayed on the screen.
- To scroll this area, use the arrow keys. Turn Num Lock off!
- To zoom out and in on the design area, use the < [Shift + ,] and > [Shift + .] keys.
- To return to the center of the drawing area, press the HOME key.
- Diglog also has nine circuit drawing “pages”.
- By default, the program starts on page 1.
- To access other pages, use the number keys.



Cursor Modes

- Bottom right hand word (in green box) is the mode.



- ROT – Rotates the gate.
- MIR- – Reflects the gate horizontally.
- MIR| – Reflects the gate vertically.
- CNFG – Configures special gates when you click on them.



Editing Menu

- Delete, Move, Copy
 - Click an option in the Editing menu
 - Drag a box around a group of gates.
 - That group will then be deleted, moved, or replicated and moved based on the option selected.
- Paste - Pastes the last thing that was copied to wherever you click.
- Implicit Move and Copy
 - Without using the edit menu, you can draw a box around a circuit.
 - Your next click will move that circuit to a new place.
 - All subsequent clicks will copy it



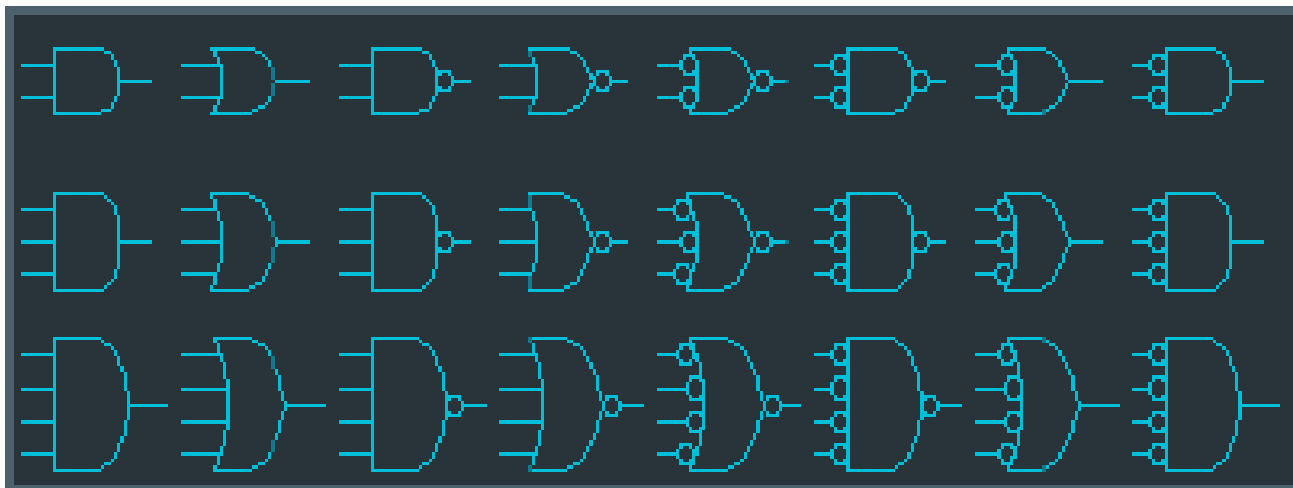
Advanced Gates

- Gates from the Catalog CAT at the bottom left of the mylib screen.
- It will load a catalog of gates on your screen.
- Click and hold the gate that you want and you will be able to place it in your circuit.
- You can also click and drag it onto the bar at the bottom of the screen next to the standard gates for quick usage.
 - Note: once you do this, there's no way to remove the gate from the bottom of the screen except restarting Diglog.



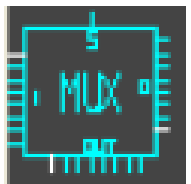
Advanced Gates

- Variations on Standard Gates
 - Multiple levels of inputs so you don't have to waste time creating and/or trees
 - Various types of negations (little circles)

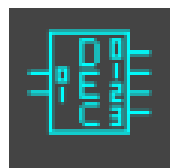




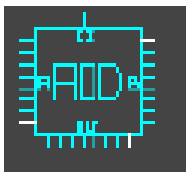
More Advanced Gates



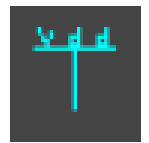
- MUX (8-bit Multiplexer) - S selects the output: input 0 or input 1.



- DEC (2 to 4 decoder) - Use the lefthand side bits 0 and 1 to chose which of the right-hand side wires is high.



- ADD - Wire the addends into A and B and wire the Carry-In bit into CI. The output will come through out. The white wires are the low order bits.



- VDD – Constant output of 1

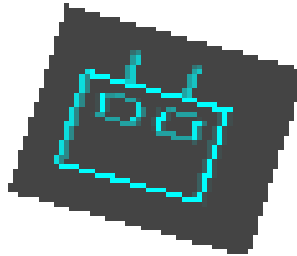


- GND – Constant output of 0



Still More Advanced Gates

- Clock



- Has two outputs which alternate between low and high.
- To change the clock rate, change to CNFG mode and click on the clock.
- Look in the newcrt window to change the Rate.
 - 10 second clock cycle means the lock is high for 5 seconds and then low for 5 seconds and so on..
- Other advanced gates will be described when you need them!



Final Reminders

- For more help, use the inline help in Diglog (at the bottom left), ask a TA, or post to the mailing list.
- These slides will be posted on the site.
- ***VERY IMPORTANT***: QUIT PROPERLY WHEN YOU ARE DONE!
- Don't forget to turn off simulate when you are not using it.



Additional Information

- Only homework problems that explicitly say a Diglog file must be handed in require the use of Diglog. If you see “Hand in a separate Diglog file for this,” submit it electronically only. Otherwise, do it by hand and submit it to the handin bin.
- Diglog source: cs.berkeley.edu/~lazzaro/chipmunk/



Misc Notes

- High impedance effects different component in different ways. For example, feeding high impedance into a flip flop sets the flip flop to 1, regardless of the clock. You're better off making sure high impedance values are not being used for anything important.
- Testing circuits with I/O wires: consider added a switch to determine whether the wires will be used for input or output. This is not a requirement when handing in circuits.



ROM Notes

- ROM input: the number on the left is the address offset in hexadecimal, while the numbers on the right are the things output at that address, in hexadecimal.
 - Example:
 - 0000:AABBCCDDEE000000000000000000000000
 - 0010:120034005600780000000000000000000000
 - Address 0x00 outputs AA, and address 0x10 (16 in decimal, 00010000 in binary) is 12. 0x01 is BB, 0x02 is CC, etc... 0x11 is 00, 0x12 is 34, etc.
- ROM config: you need to set the conf every time you reopen diglog. One of the options in the config dialog is "Save in circuit file?"



RAM Notes

- To write to RAM: Turn R off. OE doesn't matter.
- To read from RAM: Turn R on, turn OE off.
- To release high impedance from RAM: Turn R ON, turn OE on.
- The I/O wires are distinguishable because there are 8 of them -- there are several more address wires.
- Make sure every input has a value. A common mistake is to simply ignore the 5 highest bits of the address (which you don't use), rather than grounding them.



RAM Notes (cont.)

- I/O wires are shared, you so need to be very careful to:
 - avoid a race condition
 - avoid writing high impedance, which will cause undefined behavior.
- RAM reads/writes when the clock is low.
- When the clock is high, output is disabled.