LETTERS

A 160-kilobit molecular electronic memory patterned at 10^{11} bits per square centimetre

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The primary metric for gauging progress in the various semiconductor integrated circuit technologies is the spacing, or pitch, between the most closely spaced wires within a dynamic random access memory (DRAM) circuit[1]. Modern DRAM circuits have 140 nm pitch wires and a memory cell size of 0.0408 μm^2. Improving integrated circuit technology will require that these dimensions decrease over time. However, at present a large fraction of the patterning and materials requirements that we expect to need for the construction of new integrated circuit technologies in 2013 have 'no known solution'[1]. Promising ingredients for advances in integrated circuit technology are nanowires[2], molecular electronics[3] and defect-tolerant architectures[4], as demonstrated by reports of single devices[5–7] and small circuits[8,9]. Methods of extending these approaches to large-scale, high-density circuitry are largely undeveloped. Here we describe a 160,000-bit molecular electronic memory circuit, fabricated at a density of 10^{11} bits cm^{-2} (pitch 33 nm; memory cell size 0.0011 μm^2), that is, roughly analogous to the dimensions of a DRAM circuit[1] projected to be available by 2020. A monolayer of bistable, [2]rotaxane molecules[10] served as the data storage elements. Although the circuit has large numbers of defects, those defects could be readily identified through electronic testing and isolated using software coding. The working bits were then configured to form a fully functional random access memory circuit for storing and retrieving information.

The 'crossbar' geometry—a periodic array of crossed wires—provides a promising architecture for nanoelectronic circuitry[11–15], as was experimentally demonstrated by the Teramac supercomputer[4]. The crossbar is tolerant of manufacturing defects—a trait that becomes increasingly important as devices approach macromolecular dimensions and non-traditional (and imperfect) fabrication methods are employed. For example, Teramac had nearly a quarter of a million hardware defects and yet could be configured into a robust computing machine. The crossbar geometry is similar in structure to a two-dimensional crystal, implying that non-traditional methods can be employed for its construction[9,16,17]. The crossbar is also the highest-density two-dimensional digital circuit for which every device can be independently addressed[4]. This attribute enables the circuit to be fully tested for manufacturing defects and to be subsequently configured into a working circuit.

A few groups have reported on non-lithographic methods for fabricating crossbar circuits[16,18], but most methods are not yet feasible for fabricating more than a handful of devices. Furthermore, the assembly of nanowires into narrow-pitch crossbars without electrically shorting adjacent nanowires remains a challenge. We previously reported on the superlattice nanowire pattern transfer (SNAP) method for producing ultradense, highly aligned arrays and crossbars of high-aspect-ratio metal or semiconductor nanowires[19] containing up to 1,400 nanowires at a pitch as small as 15 nm (see Supplementary Information). We also reported on the use of bistable [2]rotaxane molecular monolayers as the storage elements within crossbar memories, using micrometre-scale wiring[20]. Here we combine these methods and materials, along with the defect-tolerance concepts learned from the Teramac supercomputer, to construct and test a memory circuit at extreme dimensions: the entire 160,000-bit crossbar is approximately the size of a white blood cell ($\sim 13 \times 13\ \mu m^2$).

The fabrication of this molecular memory circuit, which required the integration of molecular switches with large numbers of semiconductor and metal nanowires, presented a number of challenges. We needed to develop a process flow in which the [2]rotaxane molecular monolayer was incorporated into the circuit as close to the final step as possible, and then protect that monolayer during subsequent processing steps. We also had to establish electronic measurement protocols that could be used to follow the conductivity status of the nanowires during the entire nanofabrication procedure. Details of this process flow, along with the various electronic testing protocols, are presented in the Supplementary Information.

The assembled crossbar memory (Fig. 1) consisted of 400 Si bottom-nanowire electrodes (16 nm wide, 33 nm pitch; phosphorus-doped, $n = 5 \times 10^{19}$ cm^{-3}) crossed by 400 Ti top-nanowire electrodes (16 nm wide, 33 nm pitch), sandwiching a monolayer of bistable [2]rotaxanes (Fig. 2). Each bit corresponds to an individual molecular switch tunnel junction (MSTJ) defined by a Si bottom nanowire and Ti top nanowire and contained approximately 100 [2]rotaxane molecules. Electrical contacts were established to several bottom and top nanowires to allow us to test up to 180 effective bits ('ebits') from the central region of the crossbar, but only 128 were actually tested, owing to measurement constraints. Because SNAP nanowires are patterned beyond the resolution of lithographic methods[21], each test electrode contacted two to four nanowires. (Fig. 1b). We recently reported on a demultiplexer that would allow for this memory circuit to be fully tested[22]; however, implementation of that demultiplexer would have added significant complexity to an already demanding procedure, and wasn't necessary to demonstrate the viability of this circuit. The 128 tested ebits represented between 0.5–0.7% of the full 160-kilobit crossbar distributed over 6% of the circuit area

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(Fig. 1c). We believe that this relatively small portion of the crossbar is representative of the overall circuit, on the basis of results from testing four other similarly prepared circuits.

By scanning electron microscopy (SEM) inspection, the crossbar appeared to be structurally defect-free, with no evidence of broken, wandering or electrically shorted nanowires. Nevertheless, electrical testing identified a large number of defective bits and the nature of those defects. This testing was done by first applying a +1.5 V pulse relative to the Si bottom-nanowire electrodes for 0.2 s to set all bits to '1', and then reading each ebit sequentially using a non-perturbing +0.2 V bias. A −1.5 V, 0.2 s pulse was then applied to set all bits to '0'. The status of each of the ebits was again read. The 1/0 current ratios are presented in Fig. 3a. About 50% of the bits yielded some sort of switching response. Some of that response, however, may have originated from parasitic current pathways through the crossbar array. This is an inherent drawback of crossbar architectures wherein each junction is electrically connected to every other junction. The standard remedy is to incorporate diodes at each crosspoint[23], and although the molecule/Ti interface yields some rectification[24], we additionally grounded all nanowire electrodes not being used during a read or write step. We established a threshold for a 'good' bit based upon a minimum 1/0 current ratio of ~1.5. About 25% of the ebits passed this threshold. Electrical testing revealed several types of defects (Fig. 3b). The defects classified as 'switch defects' probably

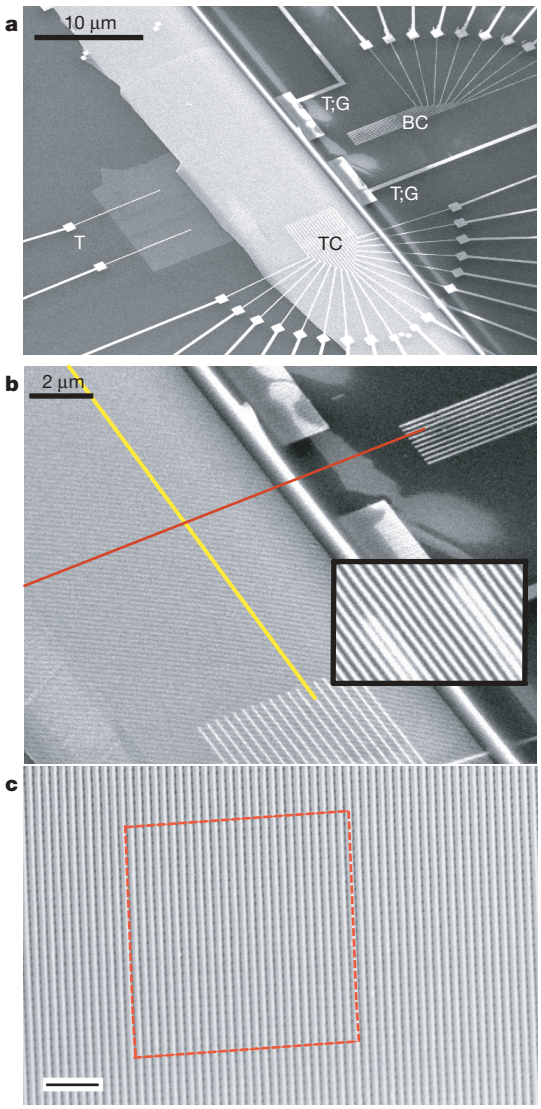

Figure 1 | SEMs of the nanowire crossbar memory. **a**, Image of the entire circuit. The array of 400 Si bottom nanowires is seen as the light grey rectangular patch extending diagonally up from bottom left. The top array of 400 Ti nanowires is covered by the SNAP template of 400 Pt nanowires, and extends diagonally down from top left. Testing contacts (T) are for monitoring the electrical properties of the Si nanowires during the fabrication steps. Two of those contacts are also grounding contacts (G), and are used for grounding most of the Si nanowires during the memory evaluation, writing and reading steps. Eighteen electron-beam-lithography patterned top contacts (TC) and ten such bottom contacts (BC) are also visible. The scale bar is 10 μm. **b**, An SEM image showing the cross-point of top- (red) and bottom- (yellow) nanowire electrodes. Each cross-point corresponds to an ebit in memory testing. The electron-beam-lithography defined contacts bridged two to four nanowires each (inset). The scale bar is 2 μm. **c**, High-resolution SEM of approximately 2,500 junctions out of a 160,000-junction nanowire crossbar circuit. The red square highlights an area of the memory that is equivalent to the number of bits that were tested. The scale bar is 200 nm.

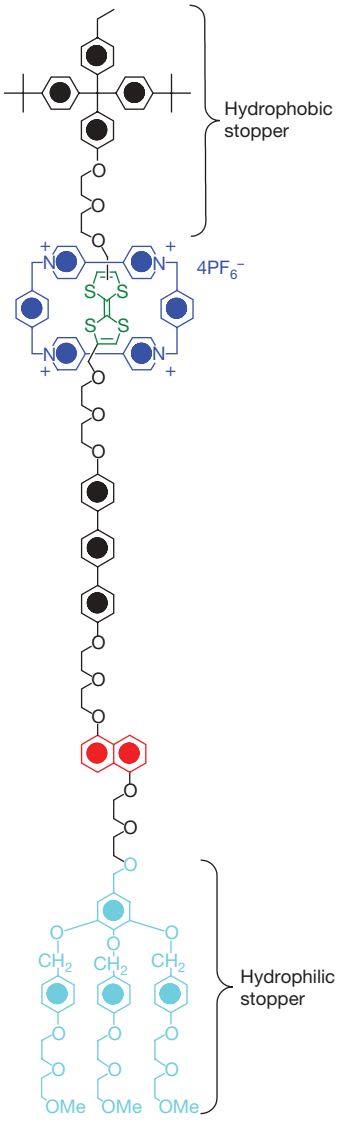

Figure 2 | Structural formula of the bistable [2]rotaxane used in the crossbar memory. The ground-state conformation is shown and corresponds to the low-conductance, or '0' co-conformation. The molecule is oriented with the (light blue) hydrophilic stopper in contact with the Si bottom-nanowire electrodes. The switching mechanism involves oxidation of the (green) tetrathiafulvalene (TTF) site to the TTF^{+1} or TTF^{+2} oxidation state, followed by translation of the blue ring from the TTF^{+} site to the (red) dioxynapthalene site. The TTF^{+} is reduced back to the TTF^{0} oxidation state to form the metastable state co-conformer, which is the high-conductance, or '1' state. The metastable state will relax back to the ground state with a half-life of about an hour.

arose from subnanometre variations in the reactive ion etching process that was used to define the Ti crossbar top nanowires. Isolated devices, or crossbar memories patterned at substantially lower densities and with larger wires, can typically be prepared with a nearly 100% yield. The switch defects led to only a proportional loss in the yield of functional bits, whereas bad contacts or shorted nanowires removed an entire row of bits from operation.

An important result from the defect map (Fig. 3b) is that the good and bad bits are randomly dispersed, implying that the crossbar junctions are operationally independent of one another. However, the ultimate test of any memory is whether it can be used to store and retrieve information. From the defect map, we identified the addresses of the usable ebits, and from those addresses configured an operational memory (Fig. 4a).

The solid-state switching signature of the bistable [2]rotaxanes that were used here has been shown to originate from electrochemically addressable, molecular mechanical switching for certain device structures[10,20], but not for metal wire/molecule/metal wire junctions[25]. In fact, our desire to use molecular mechanical bistable switches as the storage elements is what dictated our choice of the Si nanowire/molecule/Ti nanowire crossbar structure. This switching signature should be effectively size-invariant, meaning that it should scale to the macromolecular dimensions of these crossbar junctions. Solid-state-based switching materials[26,27] will probably not exhibit similar scaling since they arise from inherently bulk properties. The thermodynamic and kinetic parameters describing both the bistability and switching mechanism of the [2]rotaxane switch (and similar molecular mechanical switches[28]) have been quantified in a variety of environments[10]. Those measurements required robust switching devices that could be cycled many times and at various temperatures. The memory bits measured here were much more delicate—although all good ebits could be cycled multiple times (as shown by the testing and writing steps), most ebits failed after a half-dozen or so cycles, and none lasted longer than ten cycles. However, we measured the rate of relaxation from the 1→0 state for many of the ebits (Fig. 4b). From a device perspective, this represents the volatility, or memory retention time, of the bits. With respect to the bistable [2]rotaxane switching cycle, this represents a measurement of the rate-limiting kinetic step within the switching cycle[10]. Our measured rate (90 ± 40 min; median decay 75 min) was statistically equivalent to that reported for much larger (and more fully characterized)

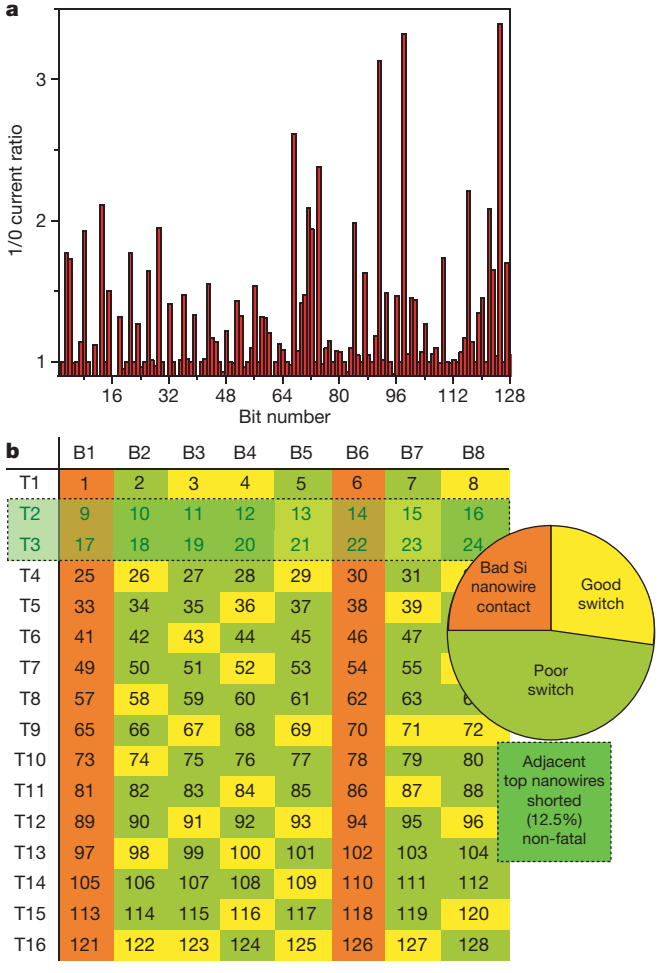

Figure 3 | Data from evaluating the performance of the 128 ebits within the crossbar memory circuit. a, The current ratio of the 1 state divided by the 0 state of the tested ebits. Note that many of the ebits exhibit little to no switching response. Those ebits are defective. **b**, A map of the defective and useable ebits, along with a pie-chart giving the testing statistics. Note that, except for the bad Si nanowire contacts on bottom electrodes B1 and B6, and the shorted top electrodes T2 and T3, the defective and good bits are randomly distributed. Poor switch defects are poorly switching or non-switching ebits that either exhibited an open-circuit conductance (26% of all ebits tested) or a conductance similar to that of a closed bit (22% of all ebits tested).

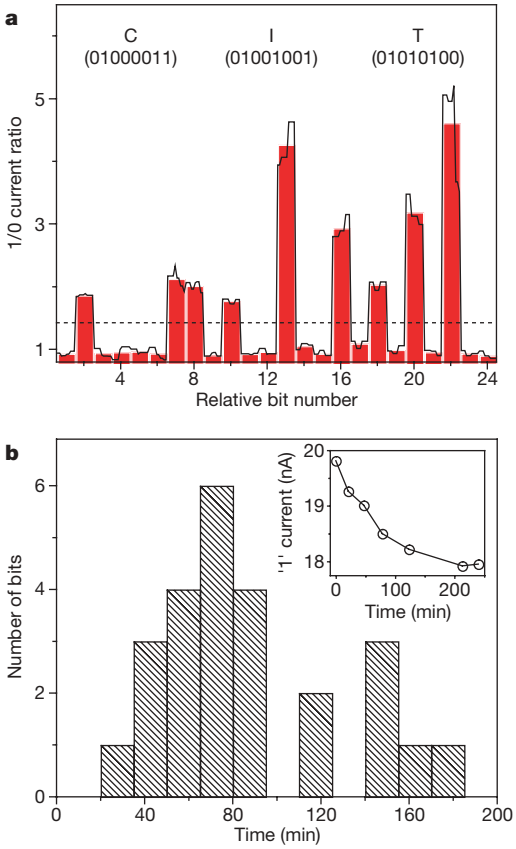

Figure 4 | Demonstration of memory storage and retention characteristics from the molecular electronic crossbar memory. a, A demonstration of point-addressability within the crossbar. Good ebits were selected from the defect mapping of the tested portion of the crossbar. A string of 0s and 1s corresponding to the ASCII characters for 'CIT' (the abbreviation for the California Institute of Technology) were stored and read out sequentially. The dotted line indicates the separation between the 0 and 1 states of the individual ebits. The black trace is raw data showing ten sequential readings of each bit, while the red bars represent the average of those ten readings. Note that deviations of individual readings from their average are well separated from the threshold 1/0 line. **b**, A histogram representing the 1/e decay time of the 1 state to the 0 state. The 25 ebits represented in the data were each large ebits, comprising approximately 100 junctions, to increase the measurement signal-to-noise ratio. Raw data from a single large ebit is shown in the inset. The solid line is a guide to the eye, not a fit.

devices (58 ± 5 min)[10]. Thus, our results are consistent with a molecular mechanism for the switching operation[10,20].

Many scientific and engineering challenges, such as device robustness, improved etching tools and improved switching speed, remain to be addressed before the type of crossbar memory described here can be practical. Nevertheless, this 160,000-bit molecular memory does indicate that at least some of the most challenging scientific issues associated with integrating nanowires, molecular materials, and defect-tolerant circuit architectures at extreme dimensions are solvable. Although it is unlikely that these digital circuits will scale to a density that is only limited by the size of the molecular switches, it should be possible to increase the bit density considerably over what is described here. Recent nano-imprinting results suggest that high-throughput manufacturing of these types of circuits may be possible[29]. Finally, these results provide a compelling demonstration of many of the nanotechnology concepts that were introduced by the Teramac supercomputer several years ago, albeit using a circuit that contained a significantly higher fraction of defective components than did the Teramac machine[4].

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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