

CS 159: Homework 4
Professor John Savage
Assigned: March 17, 2008,
Due: March 31, 2008

1. Show that a circuit for a Boolean function (one output vertex) over the standard basis can be transformed into one that uses negation only on inputs by at most doubling the number of AND, OR, and NOT gates and without changing its depth by more than a constant factor.

Hint: Find the two-input gate closest to the output gate that is connected to a NOT gate. Change the circuit to move the NOT gate closer to the inputs.

2. Over the basis B_2 derive good upper and lower bounds on the circuit size of the functions $f_4^{(n)} : \mathcal{B}^n \mapsto \mathcal{B}$ and $f_5^{(n)} : \mathcal{B}^n \mapsto \mathcal{B}$ defined as

$$\begin{aligned}f_4^{(n)} &= ((y + 2) \bmod 4) \bmod 2 \\f_5^{(n)} &= ((y + 2) \bmod 5) \bmod 2\end{aligned}$$

Here $y = \sum_{i=1}^n x_i$ and \sum and $+$ denote integer addition.

3. An **n -superconcentrator** is a directed acyclic graph $G = (V, E)$ with n input vertices and n output vertices and the property that for any r inputs and any r outputs, $1 \leq r \leq n$, there are r vertex-disjoint paths in G connecting these inputs and outputs. (Paths are **vertex-disjoint** if they have no vertices in common.)

- (a) Prove that to pebble any $S + 1$ outputs of an n -superconcentrator, $S + 1 \leq n$, from an initial placement of S pebbles requires that at least $n - S$ different inputs be pebbled.

Hint: Suppose that at most $n - (S + 1)$ inputs are pebbled from an initial placement of S pebbles to pebble $S + 1$ outputs. Can you reason from the superconcentration property that $S + 1$ or more inputs cannot remain unpebbled since $S + 1$ outputs are pebbled?

- (b) Use the result of question (a) to show that to pebble an n -superconcentrator with S pebbles in time T requires S and T to satisfy the following inequality:

$$(S + 1)T \geq \frac{n^2}{2}.$$

Hint: As in the proof of Theorem 10.4.1 divide time up into consecutive intervals. Choose the intervals so that each has the same number of outputs pebbled during it. Apply the results of the previous problem to obtain a lower bound on the sum of the number of input and output vertices that are pebbled during the interval.

4. Derive upper and lower bounds on the product $(S + 1)T$ for pebblings of circuits for the squaring function $f_{\text{square}}^{(n)}$ that are within a factor of $O(\log^2 n)$ of one another.
5. Show that the function defined by the product of three square matrices has a semiselective planar circuit size that is quadratic in its number of variables and that it can be realized by a VLSI chip with AT^2 that meets the semiselective planar circuit size lower bound.

Hint: If possible, obtain this result from known results.