Crossbar Addressing Using Core-Shell Nanowires*

Eric Rachlin, John Savage
Department of Computer Science
Brown University

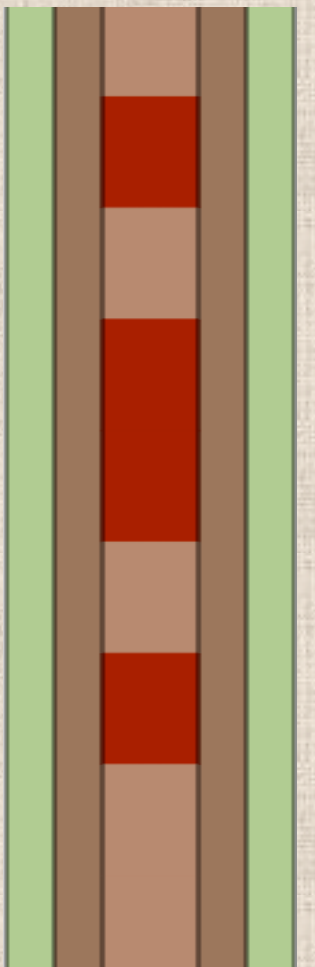
* Supported in part by NSF Grant CCF-0403674

Working with Crossbars

- Crossbars can serve as a basis for both memories and circuits.
- Nanowires can be assembled into crossbars, but assembly is stochastic.
- Nanowire crossbars must interface with lithographically produced technology.
- Core-shell nanowires provide a reliable interface by avoiding misalignment.

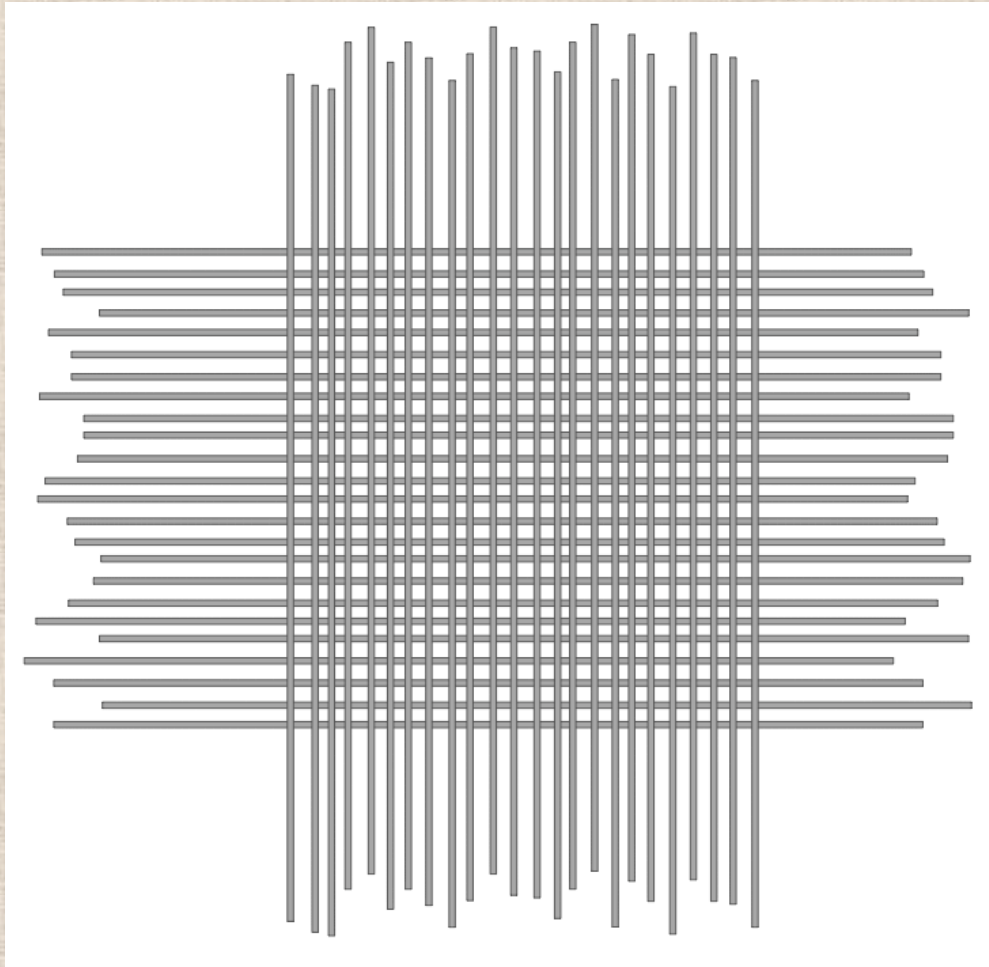
Making Nanowires with CVD

- Chemical vapor deposition grows silicon nanowires axially, then radially.
- ***Modulation-doped nanowires*** have a pattern of heavily and lightly doped regions grown along their axis.
- ***Core-shell nanowires*** have a sequence of insulating shells grown around their doped core.



Forming Nanoarrays

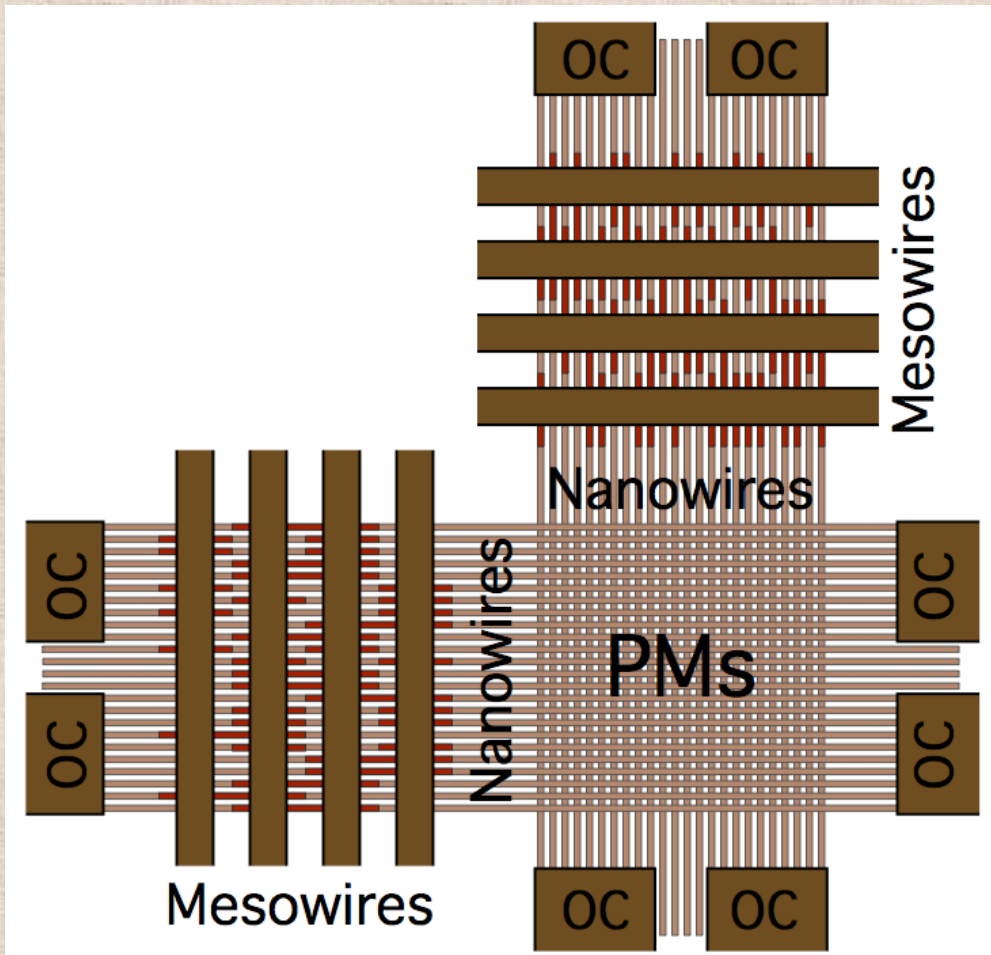
- Nanowires can be aligned fluidically then deposited in parallel.
- A layer of molecular devices is placed between two sets of perpendicular wires.
- Axial alignment is poor.



Controlling Nanoarrays

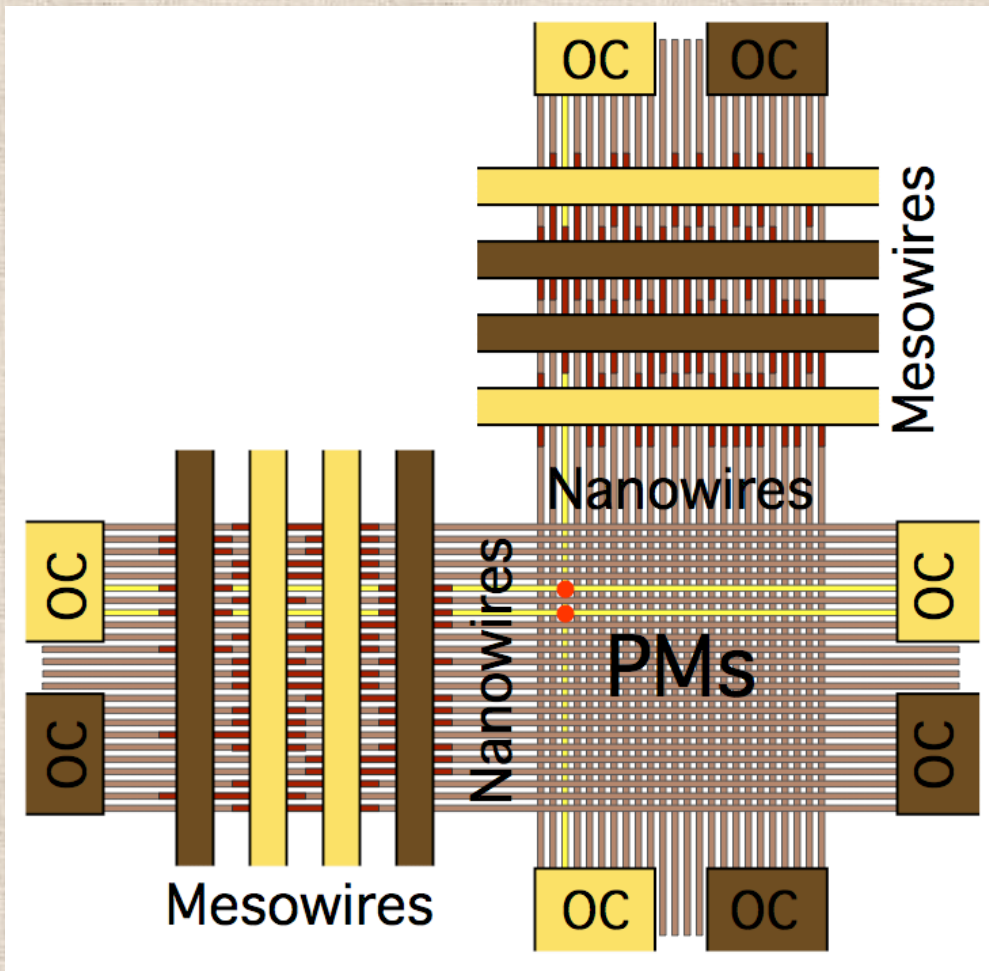
How can lithographic circuitry be used?

- ***Ohmic contacts*** apply voltages to groups of consecutive NWs.
- Mesoscale ***address wires*** turn off NWs within each group.
- NWs act as FETs.



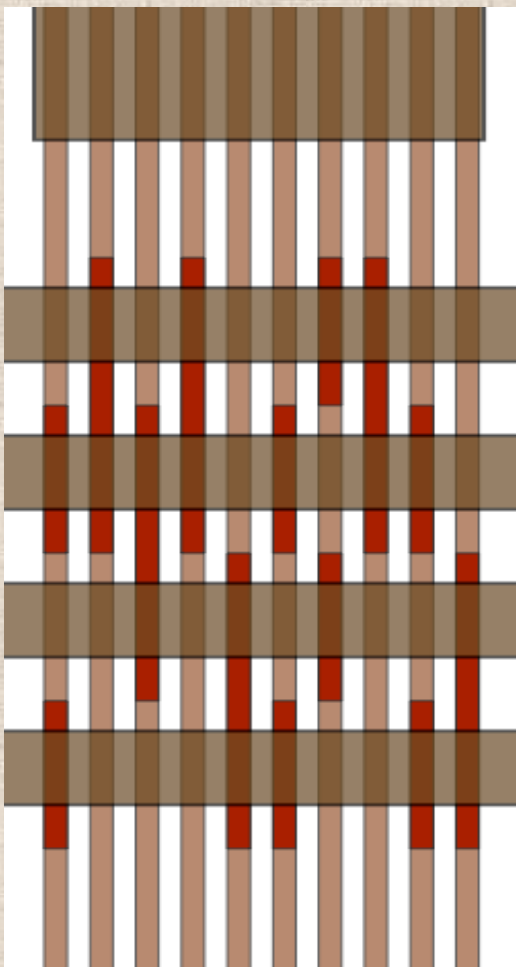
Read/Write Operations

- Pairs of nanowires provide control over molecular devices.
- Larger voltages set the conductivity of crosspoints.
- Smaller voltages measure conductivity.



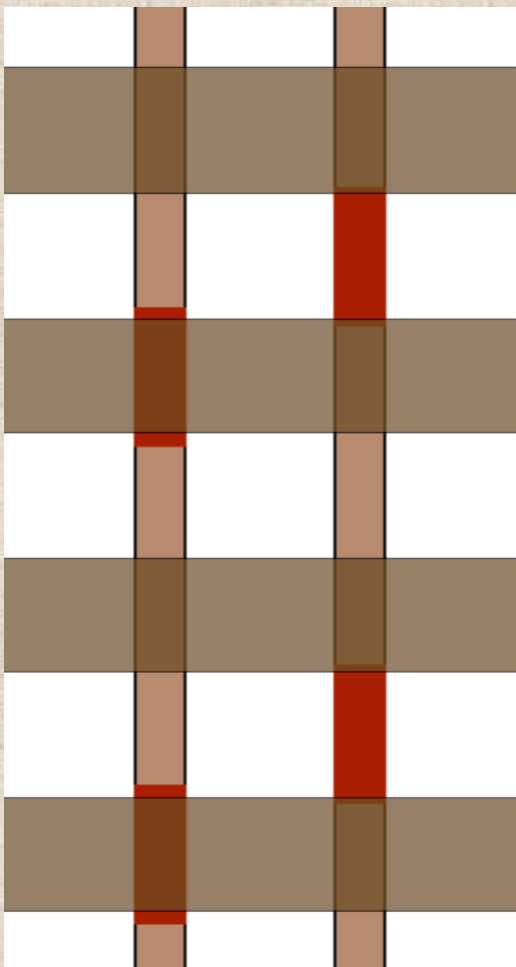
Nanowire Codewords

- An address wire turns off a NW if it is adjacent to a lightly doped region.
- A set of address wires that turn off a nanowire are called its ***codeword***.
- Codewords are randomly deposited.
- We must produce enough NW types so that many codewords are present at each contact with high probability.



Misalignment

- Modulation-doped nanowires shift axially to produce codewords.
- Shifting may cause doped regions to misalign with address wires.
- Core-shell nanowires can produce similar codewords, but without misalignment.



Core-Shell Nanowires

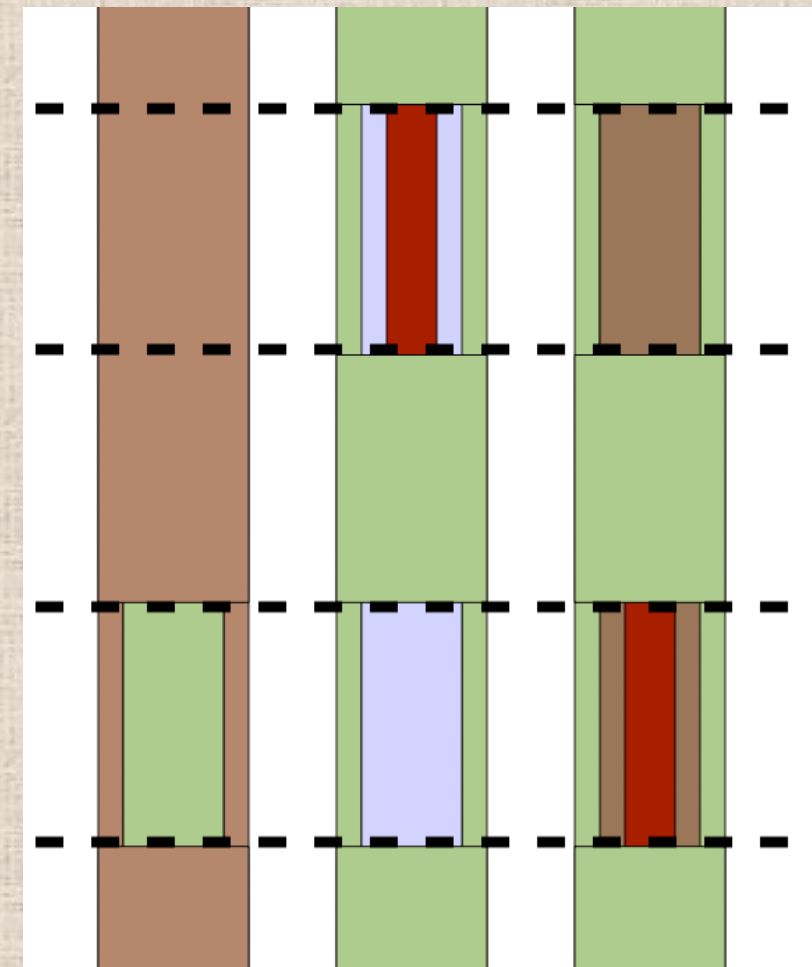
- Instead of modulation-doped NWs with many ***doping patterns*** use core-shell NWs with many ***shell sequences***.
- Create shells from ***independently etchable materials***.
- If we use n materials and k shells: $N = n\,(n-1)^{(k-1)}$ sequences are possible.

Selective Etching

- Consider NWs with the shell sequence $s_1, \ldots, s_k$. Here s_1 is the outer shell.
- Let $E(s_i)$ be the etching process that removes only material s_i.
- The etching sequence $E(s_1), \ldots, E(s_k)$ exposes only the cores of these NWs.

Linear Decoding

- Apply a different *k* step etching sequence under each address wire.
- $N = n(n - 1)^{(k-1)}$ types of nanowire are controlled using *N* address wires.
- *12* codewords will do!



Logarithmic Decoder

Can codewords be shorter?

- When $k = 1$, each type of nanowire can be etched with an arbitrary codeword.
- We can accommodate larger k if NWs are manufactured with different sets of materials in consecutive layers.
- This limits N to at most $(n/2)^k$.

Additional Possibilities

- ***Fault Tolerance:*** If codewords have sufficiently large Hamming distance, errors in etching will be tolerated.
- ***Two-Stage Etching:*** Codewords reveal which sequences are present.

  From known sequences, a second etching process can produce new codewords deterministically.

To Review…

- Core-shell nanowires generate codewords which are never misaligned!
- Linear decoding creates high density memories with only two shells!
- More sophisticated decoding permits efficient fault tolerance!