

The Systolic Array Neurocomputer:
Fine-Grained Parallelism at the Synaptic Level

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Abstract

Neural models of computing are defined in terms of large numbers of interconnected neuron-like units. These models have been implemented on various parallel processors, employing relatively coarse-grained parallelism at the level of neurons or groups of neurons. We present a new algorithm for parallelism at the synaptic level on fine-grained mesh-connected systolic arrays. The resulting system is shown to perform extremely well, computing at the rate of 300 million connections per second (CPS) during generalized delta rule learning for a multilayered neural network.

STEPS TOWARDS A VLSI IMPLEMENTATION
OF THE BACK PROPAGATION ALGORITHM:
NON-LINEAR SYNAPTIC FUNCTIONS.

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Abstract

This paper presents a theoretical modification to the Back Error Propagation (BEP) equations [1] which allows a more efficient hardware implementation to be made, when fabricating in analogue VLSI. Through simulation results it is shown how this modification affects the performance of the BEP algorithm when performing simple learning tasks.

LEARNING ON VLSI: A GENERAL
PURPOSE DIGITAL NEUROCHIP

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ABSTRACT

We present a general-purpose digital neurochip for the resolution and the learning stages of neural algorithms. It updates neuron states and synaptic coefficients in parallel on input neurons. Using a standard technology (1.6 μm CMOS), a chip may implement 32 input and 16 output neurons with 16 bit synaptic coefficients. Typical on-chip operation time is 2 μs for one neuron state or 32 coefficients updating, and with 8-bit input neurons. Moreover, many circuits can be assembled to simulate structured or large-size nets, as well as higher order nets.

By choosing adapted parameters, most of the learning rules considered so far for Neural Networks can be programmed. In particular, the error backpropagation algorithm is implemented by a simple arrangement of chips with optimal use of the chip parallelism and minimal inter-chip communications. Specification of the required precision for synaptic weights is given by theoretical arguments and numerical simulations: 16 bits per synapse should be sufficient for almost all the considered cases.

The Crossing Number for Neural Networks

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Abstract

This paper shows that high-connectivity neural networks are difficult to realize with VLSI chips. Neural networks are modeled by the composition of a family of bipartite graphs that reflect the connectivity found in applications. The number of crossings when they are embedded in the plane (their "crossing number") provides a lower bound on the area needed to realize them in VLSI. In this paper we develop lower bounds to the crossing number of neural network graphs under a few simple assumptions about the way edges are embedded in the plane. A graph that is a subgraph of many neural network graphs is the complete bipartite graph. We show that this graph has a crossing number that is at least cubic in the number of input and output vertices.